REMARKS

The claims remaining in the present application are Claims 1-2 and 4. The Title has been amended. The instant specification has been amended. Claim 3 has been cancelled, without prejudice. Claim 4 has been amended. No new matter has been added as a result of these amendments.

ALLOWABLE SUBJECT MATTER

Claim 2 is objected to as being dependent upon a rejected base claim, but indicated as allowable if rewritten to include the limitations of the base claim. The Applicants thanks the Examiner for indicating this allowable subject matter.

SPECIFICATION

The Title has been amended. The Applicants request review and approval of the amended Title. The instant specification has been amended to correct informalities. No new matter has been added as a result of these amendments.

35 U.S.C. §112

Claim 3 is rejected under 35 U.S.C. §112, ¶2. Claim 3 has been cancelled, without prejudice. As such, the rejection to Claim 3 is moot.

35 U.S.C. §102

Claims 1 and 3-4 are rejected under 35 U.S.C. §102(b) as being anticipated by Robinson et al., U.S. Patent No. 5,307,504 (hereinafter, Robinson). Claim 3 has been cancelled, without prejudice. As such, the rejection to Claim 3 is moot. The rejection to Claims 1 and 4 is respectfully traversed for the reasons below.

CLAIM 1

Claim 1 recites, in part:

> beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores,

Claim 1 recites "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed.

Robinson fails to disclose, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed. Rather, in Figure 6, Robinson illustrates an "x" instruction translated to numerous "y" instructions. Robinson may purport to disclose that state is committed for each "x" instruction, such that "x" instruction granularity is preserved during the occurrence of asynchronous interrupts. However, Applicants do not understand the "y" instructions to be speculative, as claimed.

The rejection states that Robinson must be able to handle branch instructions, but Robinson is silent as to speculating while processing a branch instruction. Thus, Robinson fails to disclose, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed.

For the foregoing rationale, it is respectfully submitted that Claim 1 is not anticipated or rendered obvious by Robinson. As such, allowance of Claim 1 is respectfully requested.

CLAIM 4

Claim 4 recites, in part:

> translating a first speculative sequence of host instructions from a first sequence of target instructions from a point in the translation or target instructions at which state of the target processor is known...
>
> committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions.

For the reasons discussed in the response to the rejection to Claim 1 based on Robinson, Claim 4 is not anticipated nor rendered obvious by Robinson because Robinson fails to teach or suggest, "committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions," as claimed.

Babaian

Claims 1 and 3-4 are rejected under 35 U.S.C. §102(e) as being anticipated by Babaian et al., U.S. Pre-Grant Publication 2002/0,092,002 A1 (hereinafter, Babaian). Claim 3 has been cancelled, without prejudice. As such, the rejection to Claim 3 is moot. The rejection to Claims 1 and 4 is respectfully traversed for the reasons set forth below.

CLAIM 1

Claim 1 recites, in part:

> beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores,

Babaian discloses that a set of recovery points are located in the binary translated code [0038]. Babaian further discloses properties of these recovery points [0039] – [0041]. However, Applicants do not understand Babaian to teach beginning the execution of a

speculative sequence of host instructions following a branch by immediately committing state and storing memory stores, as claimed.

The rejection notes the Babaian further discloses that the contents of host registers which correspond to the last dynamically preceding recovery point must be maintained until the next recovery point is reached in order to have the ability to restore the foreign (e.g., target) register's context. However, this does not teach or suggest that "state is committed and memory stores are stored at the beginning of the execution of a speculative sequence of host instructions following a branch from a first sequence of target instructions," as claimed. Rather, this cited passage suggests that information is saved from one recovery point to the next. However, as previously noted, the recovery points are neither taught nor suggested by Babaian to force a commit at the beginning of the execution of a speculative sequence of host instructions following a branch, as Applicants have claimed.

CLAIM 4

Claim 4 recites, in part:

> committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions.

For the reasons discussed in the response to the rejection of Claim 1 based on Babaian, Claim 4 is not anticipated nor rendered obvious by Babaian because Babaian fails to teach or suggest, "committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions," as claimed

Kelly

Claims 1 and 3-4 are rejected under 35 U.S.C. §102(e) as being anticipated by Kelly et al., U.S. Patent No. 5,958,061 (hereinafter, Kelly). Claim 3 has been cancelled, without prejudice. As such, the rejection to Claim 3 is moot. The rejection to Claims 1 and 4 is respectfully traversed for the reasons below.

CLAIM 1

Claim 1 recites, in part:

> beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores,

Kelly fails to teach or suggest, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed. Kelly may teach that a commit operation is performed after a sequence of host instructions executes without an exception occurring. For example, Kelly at col. 12, line 58 et seq. may disclose that a commit occurs after one or a group of target instructions has been translated and run without error. However, Kelly is silent as to, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed. For example, Kelly does not disclose that the commit occurs before a speculative sequence of host instructions that follows a branch, as claimed.

CLAIM 4

Claim 4 recites, in part:

> translating a first speculative sequence of host instructions from a first sequence of target instructions from a point in the translation or target instructions at which state of the target processor is known...

committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions.

For the reasons discussed in the response to the rejection of Claim 1 based on Kelly, Claim 4 is neither anticipated nor rendered obvious by Kelly because Kelly fails to teach or suggest, "committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions," as claimed.

For the foregoing rationale, Claims 1 and 4 are neither taught nor suggested by Robinson, Babaian, or Kelly. Therefore, Applicants respectfully solicit the allowance of Claims 1 and 4.

CONCLUSION

In light of the above listed amendments and remarks, reconsideration of the rejected Claims is requested. Based on the arguments and amendments presented above, it is respectfully submitted that Claims 1-2 and 4 overcome the rejections of record and, therefore, allowance of Claims 1-2 and 4 is earnestly solicited.

Should the Examiner have a question regarding the instant response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

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Ronald M. Pomerenke
Registration No. 43,009

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 FAX